

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A frequency divider comprising:

a first flip-flop without stacked transistors having a first clock input for receiving a clock signal, the first flip-flop further comprising a first set input and a first non-inverted output; and

a second flip-flop without stacked transistors having a second clock input for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input, a second set input coupled to the first non-inverted output, a second non-inverted output and a second inverted output, wherein the second inverted output ~~being~~is coupled to the first set input for providing an inverted output signal from the second flip-flop as feedback to the set input of the first flip-flop.

2. (Currently Amended) A frequency divider as claimed in claim 1, wherein a period of the second clock signal is of the same order of magnitude as a delay through an ~~inverter stage~~the second inverted output of the divider.

3. (Currently Amended) A frequency divider as claimed in claim 1, wherein a controllable switch is coupled to ~~the~~a first data input and to ~~the~~a third output and being controlled by ~~a~~the clock signal driving the first flip-flop.

4. (Currently Amended) A frequency divider as claimed in claim 1, wherein ~~the~~a controllable switch is coupled to ~~the~~a third output via resistive means.